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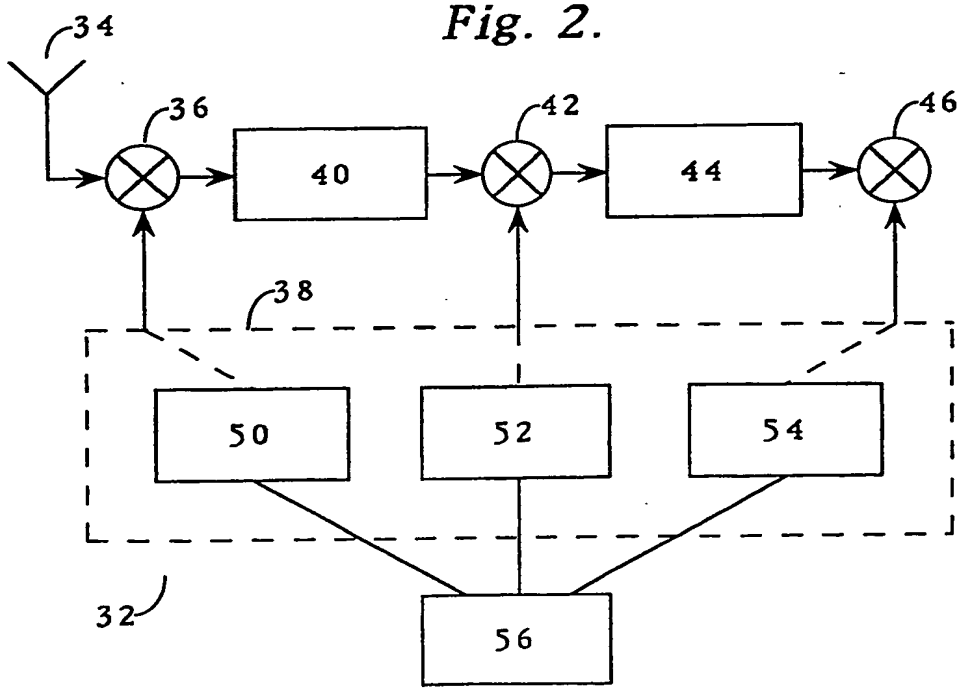
(54) Shifting spurious frequencies away from signal frequency

(57) A radio receiver 32, for use in FM, SSB and AM radio can automatically counter the internal spurious signals which are generated in the receiver by at least one internally generated signal and/or harmonics thereof: such as the injection signals generated by a radio synthesizer 38. The receiver 32 comprises means for determining frequency values of at least one internally generated signal which generate internal spurious signals for a tuned radio frequency signal and shifting means 50, 52, 54, 56, D1 for automatically shifting the frequency of the at least one internally generated signal in response to the determined frequency values so as to avoid generation of the internal spurious signals for said tuned radio frequency signal. Preferably, the determining means is in the form of a look-up table for storing predetermined frequency values which generate internal spurious signals for a plurality of radio frequency signals. In the case where two internally generated frequency signals are generated, the shifting means automatically and simultaneously shifts the frequency of both the internally generated frequency signals.

Fig. 2.



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

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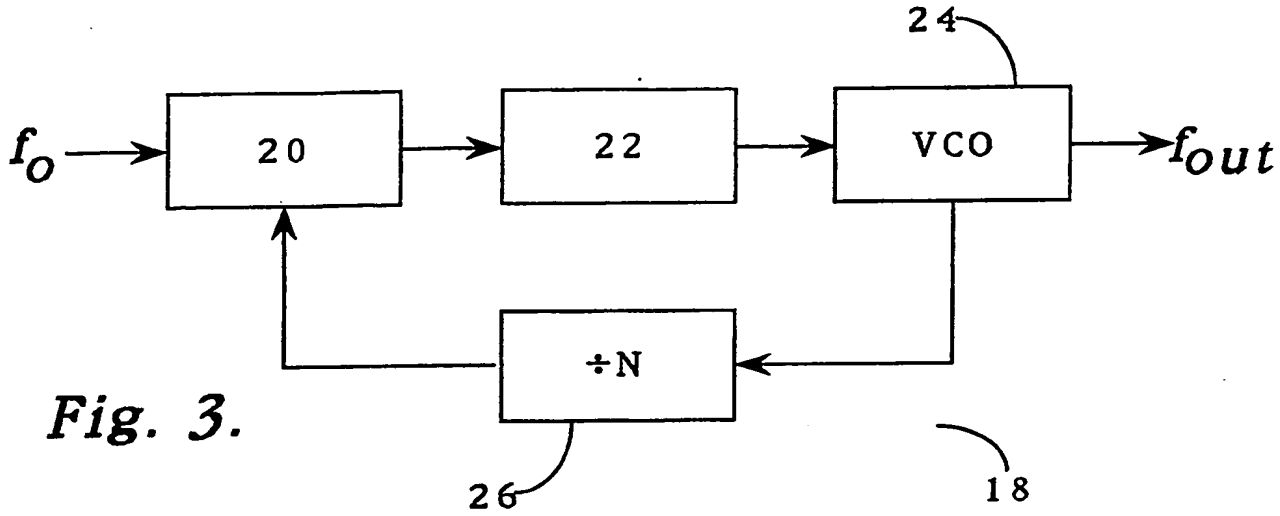

24
f_o
20
22
VCO
f_{out}
÷N
26
18

Fig. 3.

Fig. 1

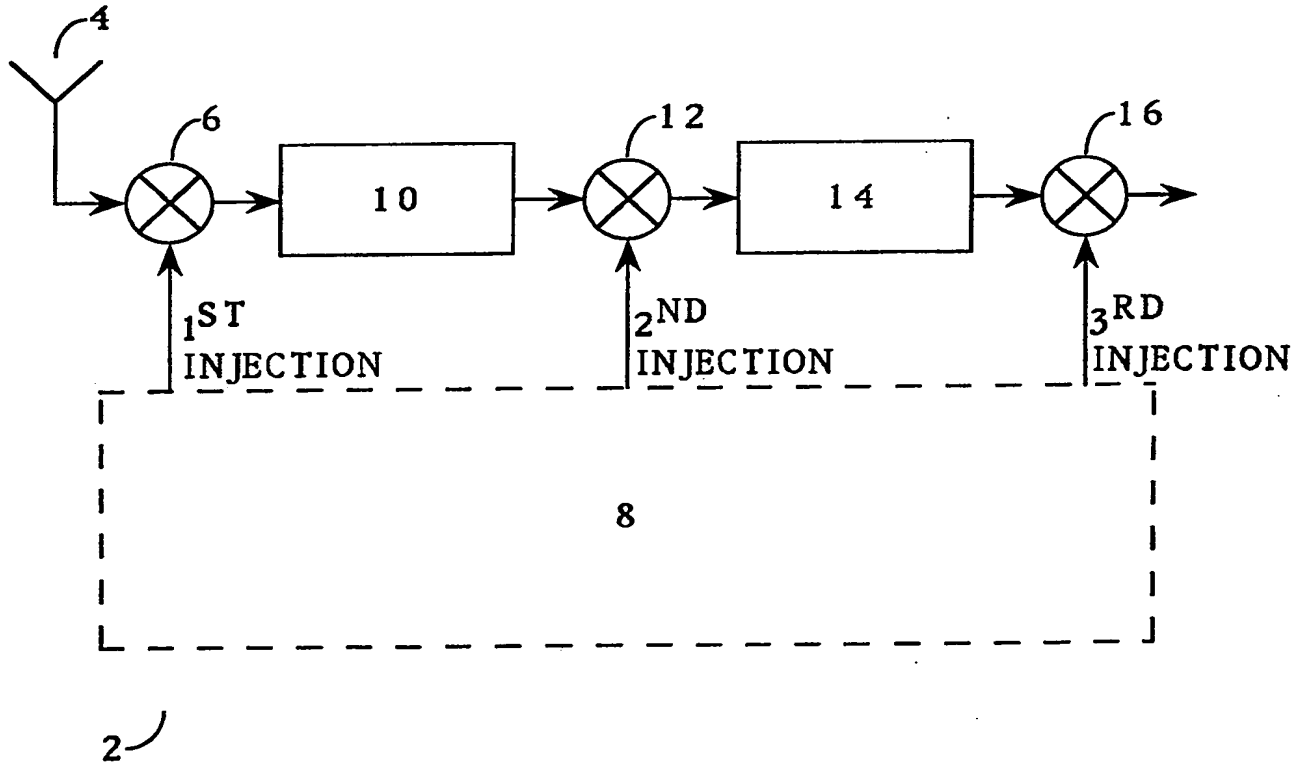
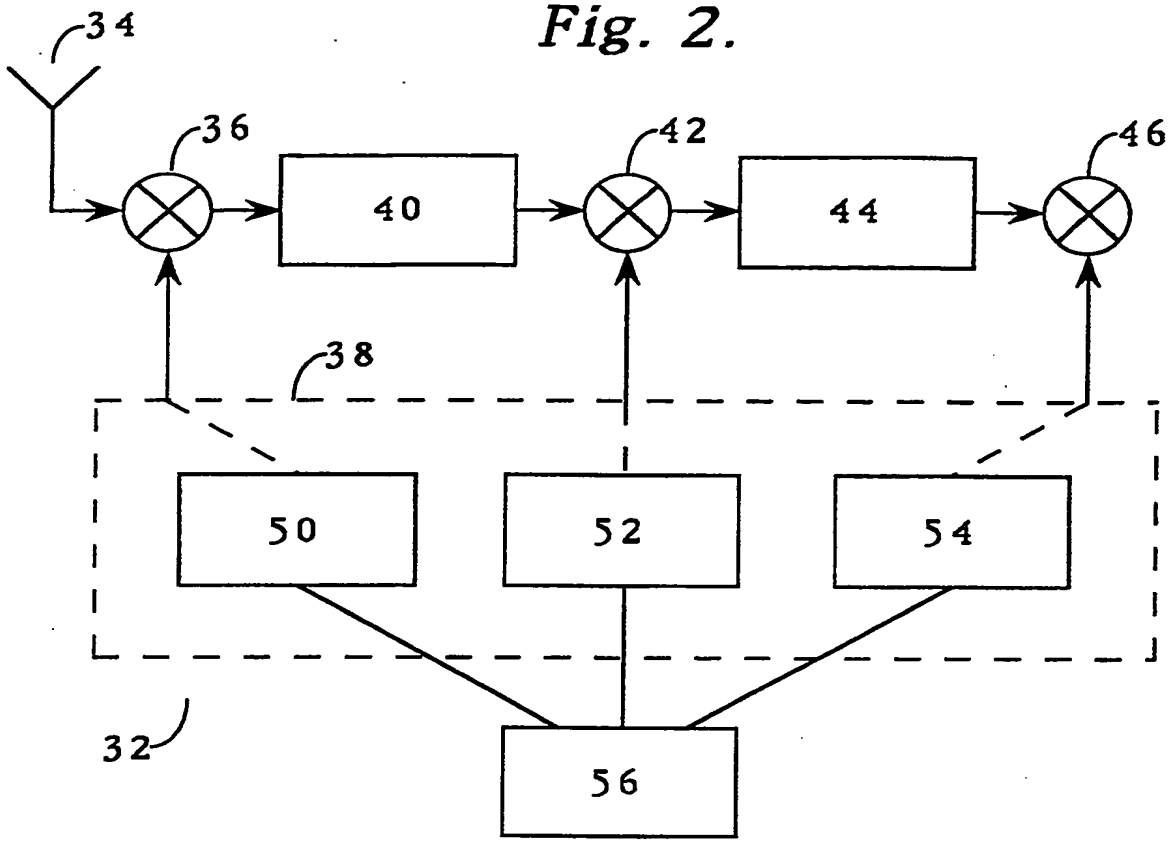

4
6
12
16
10
14
1ST INJECTION
2ND INJECTION
3RD INJECTION
8
2

Fig. 2.



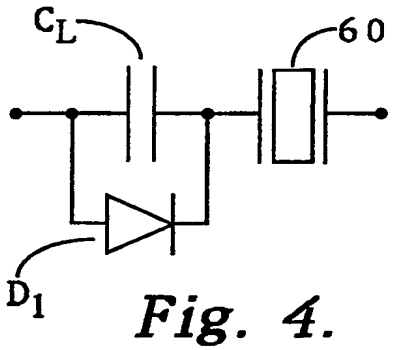


Fig. 4.

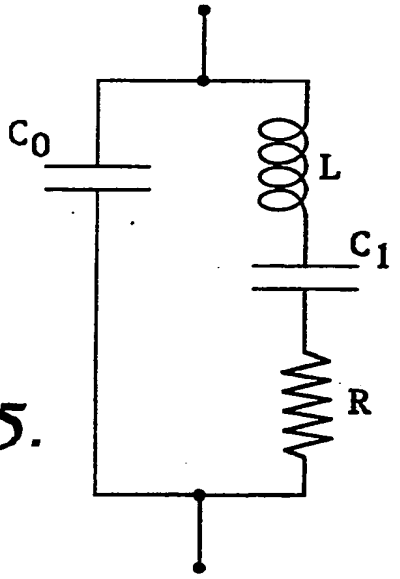


Fig. 5.

IMPROVEMENTS IN OR RELATING TO RADIO RECEIVERS

This invention relates to radio receivers and transceivers for use in FM, SSB and AM radio.

One of the most important specifications of a radio receiver is the internal spurious response of the receiver. Internal spurious signals are radio frequency (RF) signals which are generated within the receiver and which either appear at the receiver antenna or directly in the intermediate frequency (IF) path. The spurious signals create narrow band interference in the receiver passband and so can reduce the signal to noise ratio at the audio output.

Most modern radios comprise a dual conversion receiver having two IF stages and three frequency injections which are generated by a frequency synthesizer. A schematic diagram of the receive path of an SSB radio receiver is shown in Figure 1.

A frequency synthesizer 8 comprises phase locked loops (not shown) which generate first and second local injection signals and a third injection signal: the first and second injection signals are mixed in first 6 and second 12 mixers with the tuned input signal, received at the antenna 4, to produce IF signals. The third injection signal is used by a SSB detector 16 to produce the audio output signal. The outputs from first 6 and second 12 mixers are fed to first 10 and second 14 IF stages respectively.

Internal spurious can be produced in two ways: direct spurious and indirect spurious.

Direct spurious is produced from single frequency sources and appear at the antenna terminals. For example, the microprocessor, which controls the operation of the radio, requires an oscillator to clock the operation of the circuits in the radio: the microprocessor's clock can create direct spurious.

The frequency of the spurious signal for direct spurious is given by the equations:

$$F_{RF} = n F_{osc} \quad (1a$$

or

$$F_{IF} = n F_{osc} \quad (1b$$

where F_{RF} is the frequency of the received signal
F_{IF} is the frequency of the IF signal
F_{osc} is the single oscillator frequency
n is an arbitrary positive integer

Thus, if the oscillator frequency or harmonics thereof equal the frequency of the received signal or that of the IF signal, direct spurious signals are generated which produce interference in the receiver.

Indirect spurious is generated as a result of a combination between two (or more) frequency sources and appears at the IF stages. For indirect spurious the frequency of the spurious signal is given by the following equation:

$$F_{IF} = \pm QF_{1st} \pm MF_{2nd} \pm LF_{3rd} \quad (2$$

where FIF is the frequency of the IF signal
F_{1st}, F_{2nd}, F_{3rd} are the frequencies of the synthesizer injection signals
Q, M and L are arbitrary positive.integers

Thus, depending on Q, M and L, the injection signals can combine to produce spurious signals having the same frequency as the IF signals at the IF stages. The harmonics of the injection signal can therefore produce interference at the audio output.

For example, when the receiver operates at 6MHz, the first injection frequency may be 81 MHz and the second injection frequency may be 63.6 MHz. The IF frequency at the second IF stage is therefore 11.4 MHz. However, the fourth harmonic of the second injection (i.e. M = 4) and the third harmonic of the first injection (i.e. Q = 3) combine to produce a spurious signal having a frequency of 11.4 MHz: that is, the same frequency as the second stage IF signal. Hence, the spurious signal adds to the IF signal causing interference at the audio output.

In order to reduce the interference caused by internal spurious signals, radios are typically provided with a special key which allows the user of the radio to manually adjust the frequency

of the IF and clock signals. In operation, if the user hears noise at the audio output, by pressing the special key the IF and clock signals are shifted in an attempt to reduce the noise and improve the quality of the audio output. If, however, the user can still hear noise after first pressing the key, the key can be pressed again.

It is an object of the present invention to provide an improved receiver which does not require manual adjustment to reduce the internal spurious signal.

In accordance with the invention there is provided a radio receiver for receiving a tuned radio frequency signal, comprising:

means for determining frequency values of at least one internally generated frequency signal which generate internal spurious signals for said tuned radio frequency signal; and

shifting means for automatically shifting the frequency of the at least one internally generated frequency signal in response to the determined frequency values so as to avoid generation of the internal spurious signals for said tuned radio frequency signal.

Preferably the means for determining comprises storage means for storing predetermined frequency values of the at least one internally generated frequency signal which generate internal spurious signals for a plurality of radio frequency signals. The frequency values for the tuned radio frequency signal can then be read from the storage means. The storage means may be in the form of a look-up table.

The radio receiver may further comprise means for generating first and second internally generated frequency signals, such as a frequency synthesizer, whereby the shifting means is arranged to automatically and simultaneously shift the frequency of the first and the second internally generated frequency signals.

Preferably, the radio receiver further comprises a single frequency oscillator coupled serially to a capacitor, whereby the shifting means is arranged to switch the capacitor in response to the determined frequency values so as to shift the frequency of the single frequency oscillator to avoid generation of the internal spurious signals for the tuned radio frequency signal.

A receiver in accordance with the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a schematic diagram of a prior art receiver;

Figure 2 is a schematic diagram of a receiver in accordance with the present invention;

Figure 3 is a schematic diagram of a phase locked loop;

Figure 4 is a circuit diagram of a microprocessor clock in accordance with the invention; and

Figure 5 is an equivalent circuit diagram for the clock of Figure 4.

Referring to Figure 2, a receiver 32 in accordance with the present invention comprises a microprocessor 56 coupled to a synthesizer 38 and a receive path a, including an antenna 34, first 36, and second 42 mixers, first 40 and second 44 IF stages and a SSB detector 46. Like components to those of Figure 1 are referenced by the same numeral plus 30.

The synthesizer 38 comprises one or more large step PLLs. In the preferred embodiment three PLLs 50, 52 and 54 are shown but it will be appreciated that the invention is not limited thereto. The basic form of a PLL is shown in Figure 3.

The PLL 18 comprises a phase comparator 20, a low pass filter 22, a voltage controlled oscillator (VCO) 24 and a variable ratio frequency divider 26. Feedback around the phase comparator 20 is used to pull the output (f_{out}) of the VCO 24 to a frequency proportional to the frequency (f_0) of the stable reference signal supplied at an input of the phase comparator 20. When this is achieved, the loop is "locked" and the relationship between f_{out} and f_o is given by the following equation:

$$f_{out} = Nf_o \qquad (3$$

where f_{out} is the frequency of the output of the VCO 24
f_o is the frequency of the stable reference signal
N is an arbitrary integer

The frequency of the output signal f_{out} therefore depends on the variable ratio N of the frequency divider 26. N is controlled by the microprocessor 56.

The first, second and third injection frequencies are based upon the output signals from the PLLs 50, 52 and 54 respectively.

Hence, the frequency of these injection signals can be controlled by varying the variable ratio N of the respective PLLS under the control of the microprocessor 56.

All the combinations of frequencies and harmonics that create indirect spurious in the receiver for each frequency in the receiver bandwidth are stored in a look-up table, which is stored in a memory (not shown) of the microprocessor 56. The look-up table is generated using an algorithm run on a computer and the generated values are then stored in the memory. This is usually carried out at the time of manufacture. However, the look-up table may also be up-dated later to include additional combinations which are found empirically to create spurious.

The operation of the invention will now be described with reference to the example given above: that is, with the receiver tuned to 6MHz, the first injection frequency having a frequency of 81Mhz and the second injection frequency having a frequency of 63.6MHz . The IF frequency at the second IF stage is therefore 11.4 MHZ. Internal spurious appears at the second IF stage due to the fourth harmonic of the second injection signal and the third harmonic of the first injection which combine to produce a spurious signal having a frequency of 11.4 MHz.

The receiver 32 is tuned to receive 6MHz signals. The microprocessor determines the frequency of the tuned signal and uses the look-up table to determine the spurious signals which are generated for a tuned signal of 6MHz. The microprocessor uses the data read from the look-up table to determine if, and by how much, the injection signals need to be shifted and in response thereto, automatically and simultaneously shifts the first and second injection frequencies by changing the PLLs output frequency so that the new internal spurious is out of the IF bandwidth. The microprocessor 56 changes the PLL's output frequency by incrementing the ratio N in steps of one ($N \rightarrow N+1$) thereby shifting the frequencies by multiples of the smallest frequency increment (i.e. f_o).

For a stable reference frequency (f_o) of 3.8 KHz and by changing N by one, the combination of the fourth harmonic of the second injection signal and third harmonic is shifted as follows:

4x (63.6 MHz + 3.8KHz) - 3x (81MHz + 3.8 KHz) = 11.4MHz + 3.8 KHz.

The IF bandwidth of the second IF stage is 2.7KHz i.e. between 11.4MHz and 11.4027MHz. Thus, since the frequency of the combined signal is shifted to 11.4038MHz, and so out of the IF range of the second IF stage, there is no indirect spurious at the IF stages. It will be appreciated that although the injection frequencies are shifted, the overall effect is that the desired signal frequency is not changed.

The manner in which the invention prevents direct spurious will now be described.

Referring now also to Figure 4, a microprocessor clock is based upon a crystal oscillator 60 whose equivalent circuit is shown in Figure 5. The crystal oscillator in the preferred embodiment is coupled in series with a capacitor C_L which is coupled in parallel to a pin diode D1.

A capacitor C_L in series with the crystal oscillator 60 modifies the serial resonance frequency of the crystal (fs) by:

$$\Delta f = Kf_S \qquad (4$$

where Δf is the change in resonance frequency

$$K = \frac{C_1}{2(Co+C_L)}$$

The serial capacitor C_L can therefore be switched, by way of the pin diode D1 under the control of the microprocessor 56, so that the serial resonance frequency f_S of the microprocessor clock is shifted by Δf.

Thus, since direct spurious occurs when the clock frequency or the harmonics of the clock frequency is equal to the received signal frequency and/or to the frequency signals at the IF stages, by shifting the clock frequency using the serial capacitor, direct spurious can be prevented.

The frequency and harmonics of the microprocessor clock which generate direct spurious can also be stored, for each frequency in the receiver bandwidth, in a look-up table in the memory of the microprocessor 56.

In operation, when the receiver receives a signal at the antenna 4, the microprocessor 56 determines the frequencies of the spurious signals for the tuned signal by reading data from the look-up table for that tuned frequency. The microprocessor, in response to the data read from the look-up table, automatically shifts the clock frequency by way of the capacitor C_L and pin diode D1.

Although the invention has been described with reference to spurious signals generated by microprocessor clock, the same principles apply to single frequency oscillators, such as the oscillators which provide the stable reference signal to the PLLs.

It will be appreciated by those skilled in the art that although the invention has been described with reference to a receiver, the invention may also be implemented in a transceiver.

Claims

1. A radio receiver for receiving a tuned radio frequency signal, comprising:

means for determining frequency values of at least one internally generated frequency signal which generate internal spurious signals for said tuned radio frequency signal; and

shifting means for automatically shifting the frequency of the at least one internally generated frequency signal in response to the determined frequency values so as to avoid generation of the internal spurious signals for said tuned radio frequency signal.

2. A radio receiver according to claim 1 wherein said means for determining comprises storage means for storing predetermined frequency values of the at least one internally generated frequency signal which generate internal spurious signals for a plurality of radio frequency signals.

3. A radio receiver according to claim 1 or 2 wherein said radio receiver comprises means for generating first and second internally generated frequency signals, said shifting means being arranged to automatically and simultaneously shift the frequency of said first and said second internally generated frequency signals.

4. A radio receiver according to claim 3 wherein said means for generating comprises a synthesizer having at least one PLL comprising a divide by N frequency divider, said shifting means being arranged to automatically and simultaneously shift the frequency of said first and said second internally generated frequency signals by changing the value of N.

5. A radio receiver according to claim 1 or 2 further comprising a single frequency oscillator coupled serially to a capacitor, said shifting means being arranged to switch said capacitor in response to the determined frequency values so as to shift the frequency of said single frequency oscillator to avoid generation of the internal spurious signals for said tuned radio frequency signal.

6. A radio receiver according to claim 5 wherein said radio receiver further comprises a diode coupled in parallel to said capacitor.

7. A radio receiver according to any preceding claim wherein said means for determining and said shifting means comprise processing means.

8. A method of automatically reducing internal spurious signals in a radio receiver, said internal spurious signals being generated by at least one internally generated frequency signal and/or harmonics thereof, the method comprising the steps of:

receiving a tuned radio frequency signal;

determining frequency values of the at least one internally generated frequency signal which generate internal spurious signals for said tuned radio frequency signal; and

automatically shifting the frequency of the at least one internally generated frequency signal in response to said determining step so as to shift the determined frequency values to avoid generation of the internal spurious signals for said tuned radio frequency signal.

9. A method according to claim 1 wherein said radio receiver comprises storage means for storing predetermined frequency values of the at least one internally generated frequency signal which generate internal spurious signals for a plurality of radio frequency signals, and said determining step comprises:

reading the predetermined frequency values for said tuned radio frequency signal from said storage means.

10. A method according to claim 8 or 9 wherein said radio receiver comprises means for generating first and second internally generated frequency signals, and said automatic shifting step comprises automatically and simultaneously shifting the frequency of said first and said second internally generated frequency signals.

11. A method according to claim 8 or 9 wherein said radio receiver further comprises a single frequency oscillator coupled

serially to a capacitor, said automatic shifting step comprising switching said capacitor in response to said determining step so as to shift the frequency of said single frequency oscillator to avoid generation of the internal spurious signals for said tuned radio frequency signal.

12. A radio receiver substantially as hereinbefore described with reference to Figure 2 of the accompanying drawings.

13. A method substantially as hereinbefore described with reference to Figure 2 of the accompanying drawings.

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Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

Application number
9020678.0

Relevant Technical fields

(i) UK Cl (Edition K) H3Q (QCD)

(ii) Int Cl (Edition 5) H03J 5/00

Search Examiner
D MIDGLEY

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search
30 October 1990

Documents considered relevant following a search in respect of claims 1-11

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	GB 2194696A (GEN ELECT) - whole document	1-11
X	WO 84/04637A1 (MOTOROLA) - whole document	1-11

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

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E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

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